Express Mail Label
No. EJ852801423US

MEMORY CONTROLLERS HAVING PINS WITH SELECTABLE FUNCTIONALITY

Background of the Invention

This invention relates to memory controllers. More particularly, this invention relates to providing different signal functionality on the same pins of memory controller circuits.

Computer circuits typically include a CPU (central processing unit) and at least one memory controller, which controls communications between the CPU and various memory components. Computer circuits are often implemented on a printed circuit board where board space is often an important design consideration. One way to save space is to reduce the pin count on integrated circuit chip packages. One way to reduce pin count on chip packages is to reuse, where possible, the same pins for multiple purposes.

Reduction of pin count is often sought in memory controller circuits because they are generally larger chip packages. However, the advent of wide address/data paths and of numerous types of memories that need to be accommodated by memory controller circuits has resulted in an increase in the number of pins on memory controller chip packages. Moreover,

although memory controller circuits are designed to accommodate various types of memories, and can therefore be used in different types of computer circuits, such as, for example, workstations and personal computers, not all applications will include those types of memories. This may result in unused memory controller chip package pins, thus wasting valuable circuit board space.

In view of the foregoing, it would be desirable to provide a memory controller that can be coupled to different types of memories without requiring additional memory controller pins or resulting in unused pins.

Summary of the Invention

It is an object of this invention to provide a memory controller that can be coupled to different types of memories without requiring additional memory controller pins or resulting in unused pins.

In accordance with the present invention, at least some pins of a memory controller are used to provide multiple types of signals. The type of signal provided by a memory controller pin depends on the type of memory coupled to the memory controller. Clock signals and chip select signals are among the signal types that can be provided by the same memory controller pins. For example, when the memory controller is coupled to memories (e.g., buffered memory modules) that do not require as many clock signal pins as are available, the unused clock signal pins can be selected to operate as additional chip select pins. This change in functionality may allow

additional memories to be coupled to the memory controller. Selection of the functionality of memory controller pins may, for example, occur upon initialization of the memory controller in a computer circuit.

Brief Description of the Drawings

The above and other objects and advantages of the invention will be apparent upon consideration of the following detailed description, taken in conjunction with the accompanying drawings, in which like reference characters refer to like parts throughout, and in which:

FIG. 1 is a block diagram of a preferred embodiment of a memory controller coupled to unbuffered memory modules according to the present invention;

FIG. 2 is a block diagram of a preferred embodiment of a memory controller coupled to buffered memory modules according to the present invention; and

FIG. 3 is a block diagram of a preferred embodiment of a multiplexer used to select output pin functionality of a memory controller according to the present invention.

Detailed Description of the Invention

The present invention includes selectable functionality of memory controller pins that preferably depends on the type of memory used. Memory controller pins that are required when one type of memory is coupled to the memory controller may not be required when other types of memory are coupled to the memory controller. These unused pins can be advantageously

used to drive other signals, such as additional chip select signals, which can result in additional memory being coupled to the controller.

Memory modules are of at least two types: unbuffered and buffered. Unbuffered memory modules typically do not include built-in PLLs (Phase Locked Loops) or input latches. When memory controllers are coupled to unbuffered memory modules, they typically drive control, address, and data signals to each individual memory on the memory modules. When memory modules are coupled to buffered modules, registers on the buffered modules latch control, address, and data signals received by the memory modules. In addition, PLLs on buffered memory modules can reduce system loading on clocks supplied to memory modules, because the PLLs regenerate clocks for distribution to each memory on the memory modules.

Memory controllers are typically designed to accommodate a specific number of memory modules. When a memory controller is designed to accommodate a specific number of unbuffered memory modules, a corresponding number of pins are used on the memory controller to interface with the unbuffered memory modules. When the memory controller is also designed to accommodate buffered memory modules, many of the same pins used to interface with unbuffered memory modules are used to interface with the buffered memory modules as well.

However, some of the pins that interface with the unbuffered memory modules may not be required when buffered memory modules are used. For example, fewer clock signal pins may be required to interface with a

buffered memory module, because clock signals are buffered and regenerated on buffered memory modules. Pins that are left unused in buffered memory module applications are advantageously reused in accordance with the present invention.

In one embodiment of the present invention, pins that are left unused when the memory controller is coupled to buffered memory modules are constructed as dual function pins. These pins may either drive chip select signals or clock signals. When buffered memories, which require fewer clock signals, are coupled to the memory controller, the dual function pins are used as chip select pins to drive additional buffered memory modules. The reuse of memory controller pins advantageously increases the number of buffered memory modules that can be coupled to the memory controller without increasing the number of memory controller pins.

FIG. 1 shows computer system 100 which includes CPU 102, memory controller 104, and unbuffered memory modules 106 and 108. CPU 102 is preferably coupled to memory controller 104 with host bus 114. In other embodiments of the present invention, memory controller 104 is packaged in the same chip package as CPU 102. Memory controller 104 is coupled to unbuffered memory modules 106 and 108 with chip select signals 112, clock signals 116, clock signals 118 (which are provided by dual function pins 117 and 119), address bus signals, data bus signals, and other control signals (not shown). As illustrated in FIG. 1, unbuffered memory modules require one chip select signal per module and three clock signals per module.

In other embodiments, unbuffered memory modules may require two chip select and six clock signals per module, which would be provided by another embodiment of a memory controller of the present invention.

Advantageously, memory controller 104 can support twice as many buffered memory modules as unbuffered memory modules, as shown in FIG. 2. In computer system 200, memory controller 104 is coupled to buffered memory modules 206, 208, 210, and 212 with chip select signals 112 and 218 (formerly clock signals 118), clock signals 116, address bus signals, data bus signals, and other control signals (not shown). In this embodiment, buffered memory modules require one chip select signal per module and one clock signal per module. In other embodiments, buffered memory modules may each require two chip select signals and a differential clock pair, which would be provided by another embodiment of a memory controller of the present invention.

As shown in FIGS. 1 and 2, memory controller 104 can provide either clock signals 118 or chip select signals 218 at pins 117 and 119. In order to drive either clock signals or chip select signals from pins 117 and 119, clock and chip select signals are preferably multiplexed as illustrated in FIG. 3.

Multiplexer circuit 300 includes multiplexer 302 which receives chip select signal 218 and clock signal 118 as inputs. The output of multiplexer 302 is selected by a control signal 320 received from, for example, a programming register of memory controller 104. The control signal can select the chip select signal to be output to an output pin of

memory controller 104 when memory controller 104 is programmed to interface with buffered memory modules. When memory controller 104 is programmed to interface with unbuffered memory modules, the clock signal can be selected to be output to the same output pin of memory controller 104.

In another embodiment of the invention, the memory modules are DDR (Double Data Rate) memory modules. DDR memories are synchronous memories in which data access is timed with differential input clocks. DDR memories typically output data on both falling and rising edges of the input clock. A memory controller constructed in accordance with the invention can accommodate both unbuffered and buffered DDR memory modules as now described.

The differential clock inputs of unbuffered DDR memory modules can be driven by differential clock signals from dual purpose clock/chip select output pins of the memory controller. In the same embodiment, when buffered DDR memory modules are coupled to the memory controller, fewer differential clock signals are required to drive the buffered DDR memory modules. For example, three pairs of differential clock signals may be required to drive each unbuffered DDR memory module, as opposed to one pair for each buffered DDR memory module. In accordance with the invention, the unused differential clock signal pins can be programmed to be chip select signal pins. This programming (or selection) can occur, for example, upon memory controller or system initialization. The additional chip select signal pins can then be used to accommodate additional buffered DDR memory modules. For example,

if two chip select signals are required for each DDR memory module (unbuffered or buffered), two pairs of unused differential clock signal pins may result in the accommodation of two additional buffered DDR memory modules.

Thus it is seen that memory controllers are provided that can accommodate different types and numbers of memories without increasing the number of memory controller pins needed or resulting in unused pins. One skilled in the art will appreciate that the present invention can be practiced by other than the described embodiments, which are presented for purposes of illustration and not of limitation, and the present invention is limited only by the claims which follow.